REMARKS

Applicant respectfully requests allowance of the subject application. Claims 1-35 are pending. Claim 1-11 in the present application correspond to claims 1-11 in the parent application. Claim 12 in the present application corresponds to Claim 14 in the parent application. Claims 20-23 in the present application correspond to claims 23-26 in the parent application. Rejections that were asserted by the Office in the *Office Action Dated September 10, 2003* of the parent case will be addressed in reference to the corresponding claims in the present application. In view of the following remarks, Applicant respectfully requests that the rejections be withdrawn and the application be forwarded along to issuance

35 U.S.C. § 112

Claims 13 and 14 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 13 and 14, as included in the present application, have been rewritten from the parent application as indicated by the Office to remove the recitation of the "not" step. Claim 13 of the present application has also been rewritten in independent form and therefore, as indicated by the Office, is allowable. Claim 14 depends from claim 13. Therefore, Applicant respectfully requests that the rejections of claims 13 and 14 be withdrawn.

35 U.S.C. § 103

Claims 1-12 and 15-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,996,690 to George et al. (hereinafter "George). The Applicant respectfully disagrees.

THE REFERENCE

George describes a communication system that includes a parity digit generator. The described purpose of the parity digit generator is for generating ECC parity digits or check digits. The parity digit generator monitors a high speed data bus and control line between a buffer manager and a tape formatter. Data that passes over the high speed data bus is simultaneously sent to the parity digit generator over a data bus. Parity digits are calculated by the parity digit generator, transferred over a data bus and stored in parity memory for future processing. The parity digit generator also controls the placement of the calculated parity digits within the parity memory. *See George, Col. 5, Lines 56-68.*

THE CLAIMS

Claim 1 recites a method of calculating parity segments comprising:

- providing a parity calculation module configured to calculate one or more parity segments, the parity calculation module being embodied as an application-specific integrated circuit (ASIC);
- with the ASIC:
    - receiving one or more data segments that are to be used to calculate one or more parity segments;

- receiving one or more parity coefficients that are to be used to calculate the one or more parity segments, wherein:
  - the one or more parity coefficients are chosen from a plurality of coefficient subsets; and
  - each said coefficient subset is classified based on a respective parity operation;
- operating on the one or more data segments and the one or more parity coefficients to provide an intermediate computation result;
- writing the intermediate computation result to one or more local buffers on the ASIC; and
- using the intermediate computation result from the one or more local buffers to calculate one or more parity segments.

Neither George, nor any of the other submitted references, alone or in combination, disclose or suggest a method in which one or more parity coefficients are received that are to be used to calculate the one or more parity segments. The one or more parity coefficients are chosen from a plurality of coefficient subsets, and each of the coefficient subsets is classified based on a respective parity operation.

Rather, George describes three methods for calculating parity digits as shown in the following excerpt:

> Calculation of the parity digits can occur by one of three methods. The first method calculates intermediate results of parity digits after each byte of data is transferred to the data sink. The second method calculates one or more intermediate result parity digits after each block of data is transferred to the data sink. The third method encodes parity digits after an entire data interval is transferred to the data sink. The first method calculates parity digits on an ongoing basis whereas, the second and third methods

> calculate parity digits after a particular segment of data is processed; a block of data by the second method and a data interval by the third method. *George, Col. 3, Lines 3 to 15.*

None of the three disclosed methods mention how the parity digits are calculated using a coefficient. Indeed, the only mention of a coefficient in George is included in the following excerpt:

> Parity(PARBLK+j-1, i)=Parity(PARBLK+j, i) XOR g(r-j) *FDBK
> where parity(PARBLK+j-1, i) is the parity memory location of the i.sup.th parity digit in the j-1th parity block, parity(PARBLK+j, i) is equal to the i.sup.th parity digit associated with the i.sup.th data byte in the +j.sup.th parity digit block; g(r-j) is equal to the coefficient of the r-j.sup.th element of the generator polynomial, and, FDBK is equal to the feedback variable determined during block 136 above. *George, Col. 20, Line 60 to Col. 21, Line 2.*

Accordingly, for at least this reason, this claim is allowable.

Claims 2-12 depend either directly or indirectly from claim 1 and are allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those recited in claim 1, are neither shown nor suggested in the references of record, either singly or in combination with one another. For example, Claim 2 recites "wherein the ASIC has multiple local memory components to hold data that is used in the calculation of the parity segments" which is neither disclosed nor suggested, alone or in combination, by any of the submitted references.

Claim 15 recites a method of calculating parity segments comprising:

- providing a parity calculation module configured to calculate one or more parity segments;

  with the parity calculation module:

- receiving one or more data segments that are to be used to calculate one or more parity segments;
- receiving one or more parity coefficients that are to be used to calculate the one or more parity segments;
- operating on the one or more data segments and the one or more parity coefficients to provide an intermediate computation result;
- writing the intermediate computation result to one or more local buffers; and
- within one clock cycle of an associated clock, receiving (a) the intermediate computation result from the one or more local buffers, (b) one or more additional data segments and (c) one or more additional parity coefficients, and operating on them to provide a result that is stored in the one or more local buffers.

Neither George, nor any of the other submitted references, alone or in combination, disclose or suggest a method which, within one clock cycle of an associated clock, receives (a) the intermediate computation result from the one or more local buffers, (b) one or more additional data segments and (c) one or more additional parity coefficients, and operates on them to provide a result that is stored in the one or more local buffers. Accordingly, for at least this reason, this claim is allowable.

Claims 16-19 depend either directly or indirectly from claim 15 and are allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those recited in claim 15, are neither shown nor suggested in the references of record, either singly or in combination with one another.

Claim 20 recites a parity segment calculation module comprising:

an application specific integrated circuit (ASIC) having at least:

- one or more result buffers for holding intermediate computation results;
- one or more mathematical operator components configured to receive data segments and coefficients associated with the data segments and operate on them to provide intermediate computation results that can be written to the one or more result buffers, wherein the coefficients are chosen from a plurality of coefficient subsets, each said coefficient subset is classified based on a respective parity operation; and
- one or more feedback lines, individual lines being coupled between an associated result buffer and an associated mathematical operator component, to provide an intermediate computation result to the math operator for use in calculating parity segments.

Neither George, nor any of the other submitted references, alone or in combination, disclose nor suggest coefficients that are chosen from a plurality of coefficient subsets, each of the coefficient subsets being classified based on a respective parity operation. As previously stated, George merely discloses three methods of calculating a parity digit. Accordingly, for at least this reason, this claim is allowable.

Claims 21-23 depend either directly or indirectly from claim 20 and are allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those

recited in claim 20, are neither shown nor suggested in the references of record, either singly or in combination with one another.

Claims 24-35 are allowable as reciting features that are neither disclosed nor suggested in the references of record.

Conclusion

All of the claims are in condition for allowance. Accordingly, Applicant requests a Notice of Allowability be issued forthwith. If the Office's next anticipated action is to be anything other than issuance of a Notice of Allowability, Applicant respectfully requests a telephone call for the purpose of scheduling an interview.

Respectfully Submitted,

Dated: 12/4/03

By: _____

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